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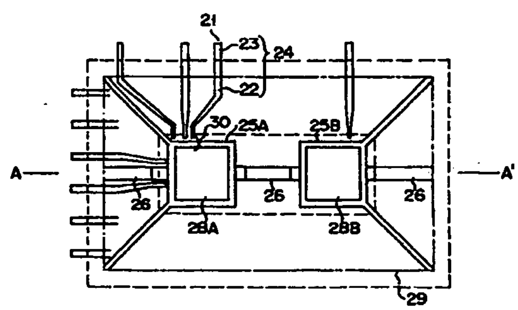
(71) Applicant: Kabushiki Kaisha Toshiba
72, Horikawa-cho Saiwai-ku
Kawasaki-shi(JP)

(72) Inventor: Sako, Shigeki, C/o Intel. Prop. Div.,
K.K. Toshiba
1-1 Shibaura 1-chome, Monato-ku
Tokyo 105(JP)

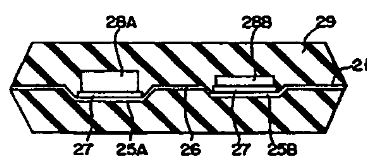
(74) Representative: Lehn, Werner, Dipl.-Ing. et al
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4e 4
D-8000 München 81(DE)

(54) Plastic molded type semiconductor device.

(57) A plurality of leads (24) and two islands (25A, 25B) are arranged on a lead frame (21) made of a conductive metal. Semiconductor chips, substrates of which have different thicknesses, are mounted on the two islands (28A, 28B), and the lead frame is bent and formed such that the chip mounting surfaces of both the islands (25A, 25B) are lower than the upper surfaces of the corresponding leads by different amounts.



F I G. 3



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PLASTIC MOLDED TYPE SEMICONDUCTOR DEVICE

The present invention relates to a plastic molded type semiconductor device and, more particularly, to a semiconductor device including a package having a thin plastic molding layer.

In recent years, an IC device having a high degree of integration is utilized in various fields. The IC device is required to be compact. An IC generally has a shape suitable for surface mounting. In order to cope with the above actual situation, an IC device having a large number of pins is required in accordance with a remarkable increase in integration density of elements. Therefore, various developments are performed.

As a part of the developments, a plastic molding material has been improved. A concept of a Bare Chip is incorporated in an assembling step of a semiconductor element and especially in a plastic molding step.

A lead frame method mainly performed as an assembling step of a semiconductor element has been frequently applied to a DIP (Dual In Line Package) type IC device having a large number of pins or an SIP (Single In Line Package) type IC device or the like.

A lead frame of a given type has a frame obtained by punching or photoetching a conductive metal thin plate and a plurality of leads which extend from the edge to the center of the frame and the distal ends of which are free distal ends. An island for mounting a semiconductor chip such as a semiconductor integrated circuit chip is formed near the distal free ends of the leads. The island and the plurality of leads are formed by a punching process or a photoetching technique at the same time as the formation of the frame.

The number of semiconductor chips which can be mounted on one island is limited. For this reason, a large number of islands each having an area in which a semiconductor chip can be mounted are formed, and a lead frame on which a plurality of semiconductor chips can be fixed is developed. Using this lead frame, a hybrid system module product in which a desired electric circuit is constituted by a plurality of chips is commercially available.

In an assembling step using a lead frame, a semiconductor chip must be electrically connected to a lead prospectively serving as an inner lead. For this reason, a pad formed on the semiconductor chip and made of a conductive metal plate electrically connected to a active element or a passive element is electrically connected to the lead through a metal thin wire by a bonding method or an ultrasonic bonding method. A flat plate-like lead frame in which a plurality of leads and an island are arranged on the same plane is usually used. In some cases, a lead frame in which a mounting surface of the island for the semiconductor chip is lower than the upper surface of another lead, i.e., a so-called depressed type or island down type lead frame may be used.

Fig. 1 is a conventional IC device using a normal flat plate-like lead frame. Referring to Fig. 1, reference numeral 11 denotes a lead frame. Two islands 12A and 12B are formed on the lead frame 11. Semiconductor chips 14A and 14B are respectively mounted on the islands 12A and 12B through an adhesive 13. Reference numeral 15 denotes a package made of a molding plastic. Note that, in Fig. 1, a metal thin wire connected by a bonding method is omitted.

Fig. 2 shows a conventional IC device using an depressed type or island down type lead frame. In the IC device, reference numeral 11 denotes a lead frame; 12A and 12B, islands; 13, an adhesive; 14A and 14B, semiconductor chips; and 15, a package.

Connection between each pad on a semiconductor chip and the corresponding lead by a thermo-compression bonding method or an ultrasonic thermo-compression bonding method is performed in the following manner. Each metal thin wire held by a bonder serving as a bonding device is compressed and thermally bonded on, e.g., the corresponding pad at the end of a tool at a predetermined temperature in a predetermined atmosphere, and the tool is moved along a predetermined track on the lead to bond the line to the lead by wedge bonding. As a result, a loop-like metal thin wire is connected between both the thermal bonding points.

In the IC device in Fig. 2, a mounting surface of each island is arranged to be uniformly lower than the upper surface of a lead by 0.15 mm to 0.2 mm.

After mounting a semiconductor chip on an island, a package having predetermined outer dimensions is formed through a plastic molding step by a transfer molding method. In this step, a pair of upper and lower metal molds are set on a plastic molding device, a lead frame is stored in a cavity formed in the lower metal mold, and a molten molding plastic is flowed inside the cavity. Arrows in Figs. 1 and 2 represent paths along which the molten molding plastic flows in the cavity.

There is a semiconductor chip in which a current is supplied in a direction of the thickness of a semiconductor substrate. Electric characteristics of this semiconductor chip is affected by the thickness of the semiconductor substrate. For this reason, in this semiconductor chip, the thickness of

the semiconductor substrate is changed in accordance with its characteristics. Therefore, when each chip mounting surface of all islands is uniformly lower than the upper surface of the corresponding lead, the following drawback occurs during a plastic molding step. That is, semiconductor chips having different thicknesses are mounted on a plurality of islands, a lead frame is stored in a cavity, and a molding plastic flows in the cavity. At this time, differences in flow rate and speed of the molten molding plastic between upper and lower portions occur within the cavity with respect to the lead frame as the center. Therefore, unsatisfactory filling of the plastic occurs. This phenomenon becomes conspicuous when the thickness of the plastic molding layer, i.e., the thickness of the package is smaller than 1.5 mm.

This unsatisfactory filling of plastic causes not only degradation of an outer appearance of the package but formation of a void inside the package. The void generates a thermal stress and causes to disconnect the metal thin wires bonded by the thermal bonding method. In addition, the void allows entrance of moisture to degrade a moisture resistance.

Thus, the unsatisfactory filling of the plastic causes degradation of reliability of a semiconductor device.

It is, therefore, an object of the present invention, there is provided a highly reliable plastic molded type semiconductor device which has a plurality of islands on which semiconductor chips are mounted and mounting surfaces of the islands lower than the upper surface of leads, wherein, when semiconductor chips having different substrate thicknesses are mounted on the islands, unsatisfactory filling of a molding plastic or formation of voids in a molding plastic constituting a package do not occur.

According to the present invention, there is provided a plastic molded type semiconductor device comprising a flat plate-like lead frame made of a conductive metal, a plurality of islands a surface of each of which is lowered from that of the lead frame by a predetermined amount upon bending of one part of the lead frame so as to lower the plurality of islands from the other part of the lead frame, a plurality of semiconductor chips respectively mounted on the plurality of islands and constituted by semiconductor substrates each having a predetermined thickness, and a package for burying and molding the semiconductor chips and made of a plastic material, wherein a lowering amount of the surface of each island from the lead frame is determined in accordance with a thickness of the substrate of each semiconductor chip.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a sectional view showing a conventional device;

Fig. 2 is a sectional view showing another conventional device;

Fig. 3 is a plan view a semiconductor device according to the first embodiment of the present invention;

Fig. 4 is a sectional view showing the semiconductor device according to the first embodiment of the present invention;

Fig. 5 is a plan view showing a semiconductor device according to the second embodiment of the present invention; and

Fig. 6 is a sectional view showing the semiconductor device according to the second embodiment of the present invention.

An embodiment of the present invention will be described below with reference to the accompanying drawings.

Fig. 3 is a plan view showing an arrangement of a semiconductor device according to the first embodiment of the present invention in which a plastic molded type semiconductor device according to the present invention is applied to a QFP (Quad Flat Package) type IC device. Note that, in the device shown in Fig. 3, a boundary of a package made of a plastic is represented by an alternate long and short dashed line, and Fig. 4 is a sectional view showing the device taken along a line A - A′ in Fig. 3.

In Figs. 3 and 4, reference numeral 21 denotes a lead frame obtained by punching or photoetching a metal thin plate made of iron, an alloy of iron and nickel, copper, or an alloy of copper. The lead frame is constituted by a plurality of leads 24 having a plurality of inner leads 22 the distal ends of which are free ends and outer leads 23 formed integrally with the inner leads 22, and two islands 25A and 25B for mounting semiconductor chips such as semiconductor integrated circuit chips. The islands 25A and 25B are formed near the free ends of the inner leads 22.

The two islands 25A and 25B are connected to each other by a connecting portion 26. The connecting portion 26 is bent and formed to arrange a mounting surface of each semiconductor chip at a level lower than the upper surface of each of the plurality of leads 24. Two semiconductor chips such as semiconductor integrated circuit chips 28A and 28B are respectively mounted and fixed on the two islands 25A and 25B by an adhesive 27. The resultant structure is molded by a package 29 made of an insulating resin such as an epoxy-based resin material.

The chips 28A and 28B can be obtained by forming an impurity region of an opposite con-

ductivity type on, e.g., a silicon semiconductor substrate of a given conductivity type according to a known method and b forming electrodes or wirings connected to the impurity region and made of a conductive metal. The chips 28A and 28B are made of silicon semiconductor substrates having different thicknesses in accordance with characteristics of the chips. For example, each thickness falls within the range of 130 µm to 400 µm.

In the semiconductor device shown in Figs. 3 and 4, adjustment for lowering the surface of an island can be performed in accordance with the thickness of the semiconductor chip, which is a characteristic feature of the present invention. That is, the surface of the island 25A on which the semiconductor integrated circuit chip 28A having a relatively large thickness is mounted is lowered by a large amount, and the surface of the island 25B on which the semiconductor integrated circuit chip 28B having a relatively small thickness is mounted is lowered by a small amount.

A plastic molding step for forming the package 29 is performed in the following manner. For example, an insulating plastic tablet of an epoxy-based resin stored in a pot of a special-purpose molding device is compressed and melted through a cull and a runner, and the molten plastic flows through the gate of a cavity formed by a lower metal mold which stores a semiconductor chip. The thickness of the plastic package, i.e., a plastic molding layer is set to be smaller than 1.5 mm for surface mounting preparation as described above.

Electrodes or bonding pads made of a conductive metal and formed on the semiconductor chip are electrically connected to the inner leads by an ultrasonic wire bonding step or a wire bonding step performed using a metal thin wire before the plastic molding step. At this time, the metal thin wire is illustrated by reference numeral 30 in Fig. 3. At this time, a loop of the metal thin wire is formed to have a height of about 300 µm. The metal thin wire having a diameter of about 50 µm and made of gold. copper. or aluminum is generally used. When a copper thin wire is used, a lead frame made of copper or an alloy of copper must be used. Furthermore, a thermally bonding step is performed in an inert atmosphere, and it must be considered to prevent oxidation of the copper thin wire and the aluminum thin wire.

Since a lowering amount of the surface of the island is naturally limited by the formation of the loop having a height of 300 µm in the thermally bonding step and the thickness of 1.5 mm, of the plastic molding layer for surface mounting preparation, the island must have a minimum thickness of 100 µm from the surface to serve as a material having moisture resistance or a protective material. Therefore, the lowering amount of the surface of the island falls within the range of 0.2 mm. Note that a plastic molded semiconductor chip is ejected by an ejector pin arranged in a special-purpose device to separate the package from the molds, and a mark formed on the end surface of the ejector pin is embossed in the package.

Note that the present invention is not limited to the above embodiment, and various modifications can be performed. For example, in the above embodiment, the case wherein two islands are provided has been described. However, the number of islands is not limited to two, and three or more islands may be provided.

In the present invention, since a lowering amount of the surface of an island is changed in accordance with semiconductor chips having different thicknesses, in a plastic molding step, unsatisfactory filling of a plastic does not occur. Therefore, a metal thin wire is not disconnected by a thermal stress, thereby improving moisture resistance.

Fig. 5 is a plan view showing an arrangement of a plastic molded type semiconductor device according to the second embodiment of the present invention. Note that a boundary of a package 29 made of a plastic is represented by an alternate long and two short dashed line. Fig. 6 is a sectional view showing the device taken along a line B - B′ in Fig. 5. A different portion between the device of this embodiment and the device of the above embodiment shown in Figs. 3 and 4 is that a connecting portion 26 for connecting two islands 25A and 25B is cut in a half way. Therefore, the same reference numerals in Figs. 5 and 6 denote the same parts as in Figs. 3 and 4, and a detailed description thereof will be omitted.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A plastic molded type semiconductor device comprising:
a flat plate-like lead frame (21) made of a conductive metal;
a plurality of islands (25A, 25B) a surface of each of which is lowered from that of said lead frame by a predetermined amount upon bending of one part of said lead frame so as to lower said plurality of islands from the other part of said lead frame;
a plurality of semiconductor chips (28A, 28B) respectively mounted on said plurality of islands and constituted by semiconductor substrates each having a predetermined thickness; and
a package (29) for burying and molding said semiconductor chips and made of a plastic material
wherein a lowering amount of the surface of each

of said islands from said lead frame is determined in accordance with a thickness of the substrate of each of said semiconductor chips (28A, 28B).

2. A device according to claim 1, characterized in that the lowering amount of each of said islands (25A, 25B) is increased proportional to an increase in thickness of the substrate of said semiconductor chip (28A, 28B), and the lowering amount of each of said islands (25A, 25B) is decreased proportional to a decrease in thickness of the substrate.

3. A device according to claim 1, characterized in that a thickness of said package (29) is set to be not more than 1.5 mm.

4. A device according to claim 1, characterized in that a thickness of each of said plurality of semiconductor chips (28A, 28B) falls within a range of 130 µm to 400 µm.

5. A plastic molded type semiconductor device comprising:

a flat plate-like lead frame (21) made of a conductive metal;

two islands (25A, 25B) a surface of each of which is lowered from that of said lead frame by a predetermined amount upon bending of one part of said lead frame so as to lower said plurality of islands from the other part of said lead frame;

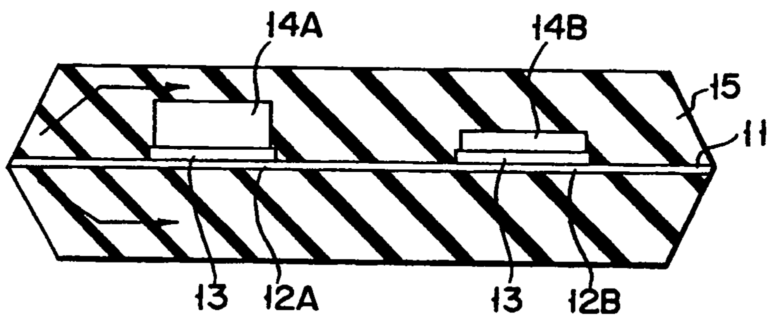
a first semiconductor chip (28A) mounted on an island having a large lowering amount from said lead frame of said two islands and constituted by a semiconductor substrate having a predetermined thickness;

a second semiconductor chip (28B) mounted on an island having a small lowering amount from said lead frame of said two islands and constituted by a semiconductor substrate having a thickness larger than that of said first semiconductor substrate; and

a package (29) made of a plastic material, for burying and molding said first and second semiconductor chips.

6. A device according to claim 5, characterized in that a thickness of said package (29) is set to be not more than 1.5 mm.

7. A device according to claim 5, characterized in that a thickness of each of said first and second semiconductor chips (28A, 28B) falls within a range of 130 µm to 400 µm.



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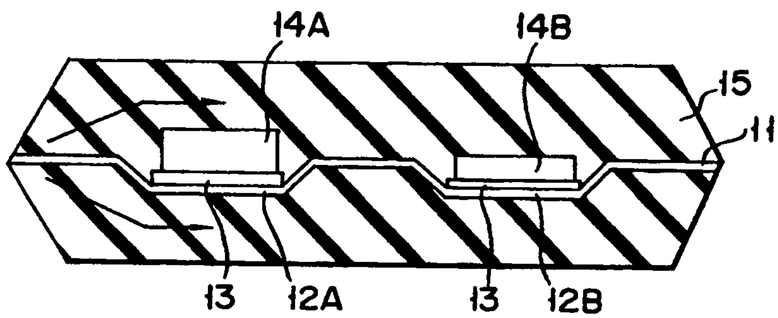

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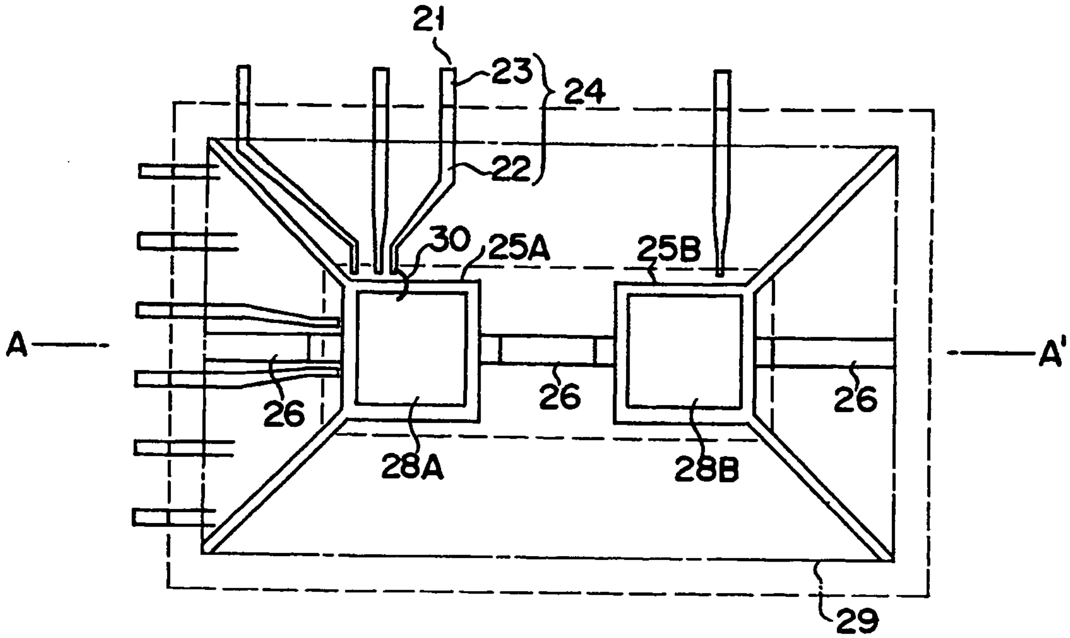
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28A
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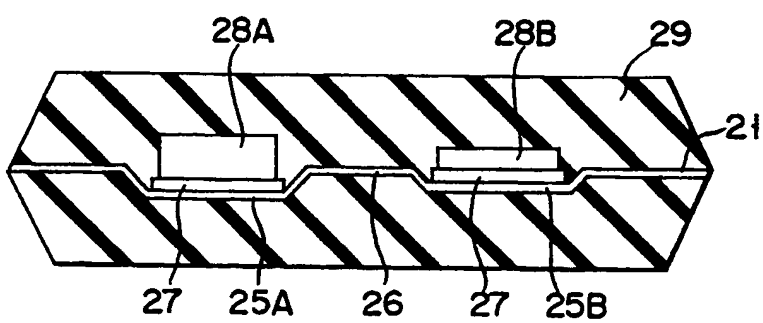
F I G. 3


28A
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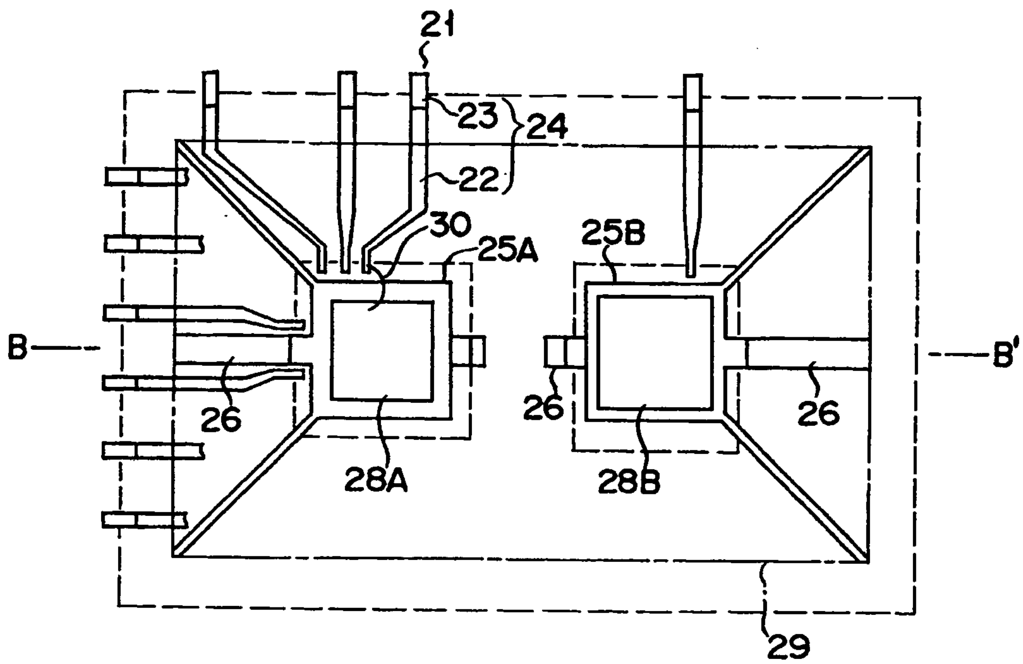
F I G. 4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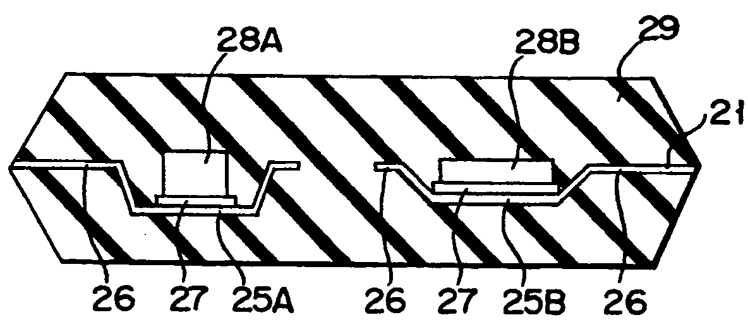
F I G. 5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F I G. 6